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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,570	06/25/2003	Koichi Nagasaki	81707.0186	3362

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EXAMINER	
FICK, ANTHONY D	

ART UNIT	PAPER NUMBER
1753	

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05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,570	NAGASAKI, KOICHI	
	Examiner	Art Unit	
	Anthony Fick	1753	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 15, 2007 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cauchy et al. (U.S. 6,103,967) in view of Fuschetti (U.S. 5,429,680).

Cauchy discloses a thermoelectric module and method of manufacturing. As shown in figure 1, the module comprises support substrates, 11 and 12, a plurality of wiring conductors formed on the opposing surfaces of the substrates, 17, 20 and 21, a plurality of thermoelectric elements, 15 and 16, and solder layers formed between the

wiring conductors and the thermoelectric elements, 26 (figure 1 and column 2, paragraph 7). The table in column 4 provides the different solder compositions disclosed by Cauchy. Solder composition 4 has good wetting and some minor voids, 1-3% surface, thus meeting the requirement of claim 1 for a 1-20% surface coverage of the voids within the solder. Figure 1 further shows the use of plated layers, 25 and 27, on the surfaces in contact with the solder layers (figure 1 and column 2, paragraph 7). The plated layers are formed from nickel (column 3, paragraphs 2 and 3). Cauchy further discloses the solder layer comprises Sn-Sb (column 3, paragraph 4 and column 4, table) and the thermoelectric elements contain at least two elements from Bi, Sb, Te, and Se (column 3, paragraph 1).

The difference between Cauchy and claim 1 is the requirement of plated layers formed with nickel and a certain thickness of gold, as Cauchy only discloses nickel-plated layers.

Fuschetti teaches a thermoelectric device as shown in figure 2 with a nickel plated layer, 31, and a gold plated layer, 32, between the solder layer and the thermoelectric element (column 3, paragraph 4). Fuschetti further teaches the thickness of the migration barrier layer or gold layer is from about 10 microinches to 150 microinches or about 0.3 microns to about 4 microns (column 4, lines 15 to 18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the gold and nickel layers including the thickness of the gold layer as in Fuschetti within the device of Cauchy because the additional layer enhances the adherence of the layers to the semiconductor and prevents migration of

metal from the solder to the semiconductor (Fuschetti column 3, paragraph 2). Because Fuschetti and Cauchy are both concerned with thermoelectric devices, one would have a reasonable expectation of success from the combination. Thus the combination meets claim 1.

Regarding claims 7 and 8, Cauchy further discloses the solder layer comprises Sn-Sb (column 3, paragraph 4 and column 4, table) and the thermoelectric elements contain at least two elements from Bi, Sb, Te, and Se (column 3, paragraph 1).

5. Claims 4 through 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cauchy in view of Fuschetti as applied to claims 1, 7 and 8 above, and further in view of Zhu (Thermal Impact of Solder Voids in the Electronic Packaging of Power Devices, 15th IEEE SEMI-THERM Symposium, 1999, pgs 22-29) and Lau et al. (Effects of Voids on Bump Chip Carrier (BCC++) Solder Joint Reliability, 2002 Electronic Components and Technology Conference, May 28-31 2002, pgs 992-1000).

The disclosure of Cauchy in view of Fuschetti is as stated above for claims 1, 7 and 8.

The differences between Cauchy in view of Fuschetti and claims 4 through 6 are the requirements of solder layer thickness, void diameter, and void shape.

Zhu teaches the thermal impact of voids on electronic devices. Figure 1a shows a multitude of small voids contained within a solder layer. Zhu further teaches an average thickness for the solder layer of 50 μm (table 1). Zhu also teaches void percentages less than 20% maintain extremely low variations in thermal transmission

through the solder (figure 4) and distributed shallow voids, like figure 1a, produce the lowest amount of thermal variations (figure 3).

Lau et al. teaches the effects of voids on solder joint reliability. Figure 4 shows the various void percentages, void sizes, and shapes tested in the study. Lau et al. teaches void sizes of 25, 50 and 75 μm (3C paragraph 1) and shows the effect these sizes have on crack formation within the solder layer (figure 14 and 3A, paragraph 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the solder layer thickness of Zhu within the device of Cauchy because the thickness is a typical thickness utilized within the art. It would have been further obvious to one having ordinary skill in the art at the time the invention was made to utilize the void diameter of Lau et al. and circular shape shown in Lau et al. and Zhu within the device of Cauchy because the void sizes and shape reduce the stress from a crack in the joint and the void can stop the crack from fracturing the solder joint, thus increasing the thermal-fatigue life of the joint (Lau et al. figure 14 and Summary and Recommendation). Also similar void percentages within the work of Zhu show the lowest thermal variations (Zhu figures 1a, 3 and 4), and the properly designed intentionally discontinuous solder joint of Lau et al. is able to maintain the device thermal resistance at an acceptable level while reducing the mechanical stress induced by the thermal expansion mismatch at the joint (Zhu Conclusions, paragraph 3). Thus the combination meets claims 4 through 6.

6. Claims 9 through 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cauchy et al. (U.S. 6,103,967) in view of Fuschetti (U.S. 5,429,680), Lau et al.

(Effects of Voids on Bump Chip Carrier (BCC++) Solder Joint Reliability, 2002 Electronic Components and Technology Conference, May 28-31 2002, pgs 992-1000) and Jafri (U.S. 4,895,606).

Cauchy discloses a thermoelectric module and method of manufacturing. As shown in figure 1, the module comprises support substrates, 11 and 12, a plurality of wiring conductors formed on the opposing surfaces of the substrates, 17, 20 and 21, a plurality of thermoelectric elements, 15 and 16, and solder layers formed between the wiring conductors and the thermoelectric elements, 26 (figure 1 and column 2, paragraph 7). The table in column 4 provides the different solder compositions disclosed by Cauchy. Solder composition 4 has good wetting and some minor voids, 1-3% surface, thus meeting the requirement of a 1-20% surface coverage of the voids within the solder. The solder has a melting point of 384°C (column 4, table).

The differences between Cauchy and claims 9 through 12 are the requirements of applying the solder paste containing a void-forming agent by heat treatment and providing nickel and gold layers with a specific gold layer thickness.

Fuschetti teaches a thermoelectric device as shown in figure 2 with a nickel plated layer, 31, and a gold plated layer, 32, between the solder layer and the thermoelectric element (column 3, paragraph 4). Fuschetti further teaches the thickness of the migration barrier layer or gold layer is from about 10 microinches to 150 microinches or about 0.3 microns to about 4 microns (column 4, lines 15 to 18).

Lau et al. teaches the effects of voids on solder joint reliability. Lau et al. teaches that voids in solder joints are unavoidable (Introduction, paragraph 4) and that these

voids are usually formed from entrapped solder flux, especially with solder pastes (Introduction, paragraph 5).

Jafri teaches formulations for soldering flux. The flux combined with the solder form a paste that is heated to join elements together in the soldering process (column 4, paragraph 1). Jafri also teaches of prior work utilizing a solder paste including a resin or paraffin wax (column 2, paragraph 3). The fluxes taught by Jafri include resins, specifically paraffin wax, with lower melting points than the solder (column 6, formula 9 and paragraph 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the gold and nickel layers with the gold layer thickness as in Fuschetti within the method of Cauchy because the additional layer enhances the adherence of the layers to the semiconductor and prevents migration of metal from the solder to the semiconductor (Fuschetti column 3, paragraph 2). Because Fuschetti and Cauchy are both concerned with thermoelectric devices, one would have a reasonable expectation of success from the combination.

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to utilize the soldering flux of Jafri within the manufacturing method of Cauchy in view of Fuschetti to form the solder layers because the fluxes provide for improved tarnish removing capability, protects and clears the base metal surfaces, and lowers the cohesive force of the solder to help in wetting the base metal surface (Jafri column 2, paragraphs 5, 6 and 7). As Lau et al. teaches the voids within solder joints are formed from entrapped solder flux, the solder flux of Jafri is a void-

forming agent producing the voids disclosed by Cauchy within the solder. Because Cauchy, Fuschetti, Jafri and Lau et al. are all concerned with solder joints, one would have a reasonable expectation of success from the combination. Thus the combination meets claims 9 through 12.

Response to Arguments

7. Applicant's arguments filed November 22, 2006 have been fully considered but they are not persuasive. Applicant argues that the combination of Cauchy and Fuschetti does not meet the claim requirements as the gold layers of Fuschetti have a thickness of about 0.001 to about 0.008 inches and this argument is applied to all the claims. The examiner respectfully disagrees. The thickness that applicant states Fuschetti is teaching corresponds to the electrically conductive layer, 35 in figure 3, that is made of copper for example (see column 5, lines 19-24). As stated above, Fuschetti teaches the gold layer thickness in column 4 to be from about 10 microinches to 150 microinches or about 0.3 microns to about 4 microns (column 4, lines 15 to 18). Therefore the cited references do teach or suggest each and every limitation of the claims as it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the same thickness of gold layer as in Fuschetti when utilizing the gold layer of Fuschetti to prevent migration of metals into the thermoelectric material. The same argument can be applied to the further combinations applied to claims 4-6 and 9-12. Therefore the rejections are maintained.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony Fick whose telephone number is (571) 272-6393. The examiner can normally be reached on Monday - Friday 7 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571) 272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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May 9, 2007

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